WHAT IS CLAIMED IS:

1. A synchronous memory system, comprising:

one or more memory modules in a main memory, with each memory module comprising one or more memory banks;

a memory control device configured to generate commands comprising a plurality of command segments with a respective plurality of elements, wherein one of the command segments is a selection command segment for selecting one or more memory banks, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment; and

a transfer bus for communication between the memory control device and the memory modules, wherein the transfer bus is in the form of a concatenated bus structure and comprises a plurality of parallel transfer lines; and wherein the memory control device is configured to transfer the commands to the memory modules using the transfer bus, and wherein the transfer bus is configured to transfer the elements of a command segment in parallel.

2. The synchronous memory system of claim 1, where the memory modules further comprise a buffer device for forwarding the commands to one or more memory banks in at least one of a respective memory module and one or more other memory modules.

3. The synchronous memory system of claim 2, where the buffer device is configured to compare the bit pattern of a given selection command segment with one or more predetermined bit patterns and to determine whether the associated command needs to be forwarded to at least one of: (i) one or more of the memory banks in the memory module; (ii) and one or more other memory modules.

4. The synchronous memory system of claim 2, wherein the buffer device is configured to generate a chip select signal for one or more memory banks.

5. The synchronous memory system of claim 1, where the selection command segment is the first segment of the commands.

6. The synchronous memory system of claim 1, wherein the number of transfer lines in the transfer bus is at least equal to the maximum number of memory banks which can be used in the memory system.

7. The synchronous memory system of claim 1, wherein the commands for each memory bank contain an element for a clock enable signal.

8. The synchronous memory system of claim 1, wherein the commands contain an element for a clock enable signal for all the memory banks.

9. The synchronous memory system of claim 1, wherein the commands for each memory bank contain an element for an on-die termination signal.

10. The synchronous memory system of claim 1, wherein the commands contain an element for an on-die termination signal for all the memory banks.

11. The synchronous memory system of claim 1, wherein the buffer device is designed to generate an on-die termination signal.

12. The synchronous memory system of claim 1, wherein the commands contain an element for a reset signal.

13. The synchronous memory system of claim 1, further comprising a transfer line connecting the memory control device and at least one of the memory modules and configured to propagate a reset signal.

14. The synchronous memory system of claim 1, wherein the commands contain an element for signaling that the command is intended for the buffer device.

15. Synchronous memory system of claim 1, wherein the memory control device comprises a coding device for coding generated commands and the buffer device comprises a decoding device for decoding received coded commands.

16. A method for communication, in a synchronous memory system, between a memory control device and one or more memory modules in a main memory using a transfer bus, where each memory module comprises one or more memory banks, the transfer bus is in the form of a concatenated bus structure and comprises a plurality of parallel transfer lines, the method comprising:

generating, with the memory control device, commands comprising a respective plurality of command segments with a respective plurality of elements, wherein one of the command segments is a selection command segment for selecting one or more memory banks, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment;

transmitting the commands to the memory modules using the transfer bus, with the plurality of elements being transferred in parallel.

17. The method of claim 16, further comprising:

receiving the commands from the transfer bus by a buffer device; and

forwarding, by the buffer device, the commands to at least one of (i) one or more memory banks in a respective memory module; and (ii) one or more other memory modules.

18. The method of claim 16, further comprising:

receiving the commands from the transfer bus by a buffer device; and

comparing a bit pattern of the respective selection command segments with one or more respective predetermined bit patterns by the buffer device; and

determining, on the basis of the comparison, whether the command needs to be forwarded to at least one of (i) one or more memory banks in a respective memory module; and (ii) one or more other memory modules.

19. The method of claim 16, further comprising:

receiving the commands from the transfer bus by a buffer device; and

comparing a bit pattern of the selection command segment with one or more predetermined bit patterns by the buffer device; and

determining, from the comparison, that the selection command segment is destined for a memory bank associated with the buffer device; and

generating, by the buffer device, a chip select signal for the associated memory bank.

20. The method of claim 16, wherein the selection command segment is transferred as the first segment of a command.

21. The method of claim 16, further comprising:

generating, by the memory control device, coded commands; and

decoding the coded command at the memory modules.

22. A protocol for communication, in a synchronous memory system, between a memory control device and one or more memory modules in a main memory using a transfer bus, where each memory module comprises one or more memory banks and the transfer bus is in the form of a concatenated bus structure and comprises a plurality of parallel transfer lines, the protocol comprising:

commands having a plurality of command segments with a respective plurality of elements and wherein one of the command segments comprises a selection command segment for selecting one or more memory banks, with each of the memory banks having at least one uniquely associated element of the selection command segment.